AICTE Sponsored
Short Term Training Program (STTP)
on
VLSI Design: Bridging Concepts to Practice

STTP-I(28.11.20 – 03.12.20)
STTP-II (28.12.20 – 02.01.21)
STTP-III (25.01.21 - 30.01.21)

Registration Form

Name:_____

_____

Designation:_____

Organization: _____

Correspondence Address:

_____

_____

_____

_____**PIN code**_____

Phone # _____

E-mail:_____

Whatsapp MobileNo_____

Category: *Academic/Industry/others*

Signature of the Participant:

Date: _____

Place: _____

Participants need to fill this registration form and upload the scanned copy in PDF format in the below registration link.

Registration Link
https://forms.gle/bqqgAjVWtMHeS3C36

Last Date for Registration*: on or before* **26th Nov., 2020**

ELIGIBILITY & REGISTRATION: No registration fee

The Faculty members, research scholars, PG students of AICTE approved Engineering colleges, Polytechnics working in the field of VLSI are eligible to apply. Admissions will be offered subject to the availability on a first-come, first-served basis & area of specialization with a maximum attendance of 100

MODE OF CONDUCTION: Online Mode – 3 times as per the dates announced, on the same theme but with different audience.

Online meeting link will be sent through Whatsapp and registered email. Since Hands on sessions will be conducted using CAD tools, all the participants are informed to get ready with their systems

CERTIFICATION:

E-Certificates will be issued to those participants who attend all the sessions of the programme and clear the online exam as per the norms stipulated by the AICTE.

Chief Patron

Capt. V. Lakshmikantha Rao, *M.P. (Rajya Sabha)*
Secretary & Correspondent, KITS Warangal (KITSW)

Patron
Sri. P. Narayana Reddy, *Treasurer, KITSW*

Chairman
Prof. K. Ashoka Reddy, *Principal*

Convener
Dr. K. Venu Madhav,
Professor & Head, Dept. of E&IE,KITSW

Coordinators
Dr. K. Sivani, *Professor, Dept. of E&IE, KITSW*
Sri O. Anjaneyulu, *Assoc. Prof., Dept. of E&IE, KITSW*
Sri B. Jeevan, *Asst. Prof., Dept. of E&IE, KITSW*

Organizing Committee
Prof. M. Sreelatha, *P**rofessor, Dept. of E&IE, KITSW***
Smt. R. Nirmala Devi, *Assoc. prof., Dept. of E&IE, KITSW*
Dr. M. Raghuram, *Assoc. prof., Dept. of E&IE, KITSW*
Sri B. Shashikanth, *Asst. Prof., Dept. of E&IE, KITSW*
Dr. K.Srinivas, *Asst. Prof., Dept. of E&IE, KITSW*
Sri B. Venumaheswar , *Asst. Prof., Dept. of E&IE, KITSW*
Smt. B.Smitha, *Asst. Prof., Dept. of E&IE, KITSW*
Smt. K.Shailaja, *Asst. Prof., Dept. of E&IE, KITSW*
Sri G,Raju, *Asst. Prof., Dept. of E&IE, KITSW*
Sri B.Krishna Sundeep, *Asst. Prof., Dept. of E&IE, KITSW*

AICTE Sponsored Short Term Training Program (STTP)

"VLSI Design: Bridging Concepts to Practice"

STTP-I (28.11.20 - 03.12.20)
STTP-II (28.12.20 - 02.01.21)
STTP-III (25.01.21 - 30.01.21)

Coordinator

Prof. K. Sivani
Dept. of EIE

Co-coordinator

Sri O. Anjaneyulu,
Associate Professor,
Dept. of EIE
+91-9440591120

Sri B. Jeevan,
Assistant Professor,
Dept. of EIE
+91-9912155777

Organized by

Department of Electronics & Instrumentation Engineering
Kakatiya Institute of Technology & Science, Warangal
(An Autonomous Institute under Kakatiya University)
(Accredited by NAAC with 'A' Grade)
Opp: Yerragattu Gutta, Hasanparthy (M),
Warangal-506015 (TS), INDIA.

Website: ***www.kitsw.ac.in***

ABOUT THE INSTITUTE

Kakatiya Institute of Technology and Science, Warangal popularly known as **KITSW**, was established in **1980** by **Ekasila Education Society (EES), Warangal,** a philanthropic society, with a primary objective of providing quality technical education. KITSW is recognized by the AICTE and also under section 2(F) and 12(B) of UGC act 1956. The UGC has granted autonomous status in 2014 under Kakatiya University (KU), Warangal. It is accredited by the NAAC with A grade (CGPA: 3.21) and all the UG engineering programmes are accredited by the NBA, New Delhi.

Located in 68 acres of lush green sprawling campus, it is one of the premier institutes of Telangana. Over the years, it has attracted academicians of proven competence onto its faculty, augmented the infrastructural facilities, modernized laboratories, placed its products in reputed organizations all over the world and thus received recognition in industry and academia. At present, it is offering UG in nine branches of engineering, PG in six engineering specializations and MBA. The KU recognized CE, ME, E&I and CSE departments as research centers for PhD programmes. The faculty at KITSW is now integrating research, innovation and incubation culture into course teaching to prepare students to gain tech skills for industry 4.0.

Warangal city is well connected to other cities by rail and road. The institute is located on Warangal - Karimnagar highway.

ABOUT ECE DEPARTMENT

The **Department of Electronics & Instrumentation (E&I) Engineering** was established in the year 1981 in Kakatiya Institute of Technology & Science (KITS), Warangal. The institute has the distinction of being the first in the country to offer a B.Tech program in Electronics & Instrumentation Engineering. Department also offers Specialized M.Tech programme in VLSI & Embedded Systems. The B.Tech program has been accredited by the National Board of Accreditation (NBA) of AICTE, New Delhi. The department is recognized as a Research center under Kakatiya University in the year 2010. The research center has state of the art research facilities which are catered to the Ph.D. scholars and PG students in the areas of Electronics, Communication, Instrumentation, VLSI and Signal Processing. Till now four research scholars are awarded with Ph.D and more are pursuing Ph.D under Department Research Center.

The department has modernized and well equipped laboratories with state of-art facilities to cater to the needs of UG and PG courses.

The list of labs available in the department is:

- VLSI Laboratory
- LIC Laboratory
- Basic Electronics Laboratory
- Microprocessor & Microcontroller Laboratory
- Measurements & Instrumentation Laboratory
- Bio-Medical& Instrumentation Laboratory
- Virtual Instrumentation Laboratory
- Process Control Laboratory
- Digital Electronics Laboratory
- Research Laboratory.

PREVIOUSLY RECEIVED FUNDS BY THE DEPT

Under the department of EIE, Prof. K. Ashoka Reddy received Rs. 8 lakh in 2009 from the AICTE toward a MODROBS on "Modernization of Measurements Lab". Prof. K. Ashoka Reddy, got Rs. 9.9 lakh research promotional scheme in 2012 from the AICTE on "Create and update general research capabilities". Prof. K. Sivani, Professor, received a MODROBS grant of Rs. 15.0 lakh on "Modernization & Automation of Process Control Laboratory," in 2019 from DST.

ABOUT THE STTP

Education in Engineering Colleges and Universities are severely lagging in meeting VLSI Industry specific needs. This creates a big gap between the Industry and the fresh engineering graduates. By conducting a Faculty Development Program, we intend to reduce this gap by training the academia on various features of VLSI System. The main focus of this program is to train the faculty on VLSI Design and VLSI Design Lab courses. This training will also be beneficial to faculty who are teaching VLSI related courses in various PG programmes and who are looking for research opportunities in the field of VLSI.

The objectives of this faculty development program are to:

- integrate a thorough knowledge on fundamentals and latest trends in VLSI Circuits with their applications.
- design and analyze the VLSI circuits and systems.
- reframe the concepts of circuit design simulation, layout design, DRC and physical verification etc.

The UG and PG programmes of Electronics and Instrumentation engineering offer various advanced courses in the field of instrumentation. VLSI is very potential area of study where students can be guided to take up projects both at UG and PG level. Hence hands-on training to the Electronics faculty of engineering colleges will make them competent to guide students on good projects/dissertations.

BENEFITS TO THE FACULTY

- Faculty will get trained in the area of Analog and digital VLSI
- Faculty will start guiding meaningful projects to UG and PG students
- Faculty will be introduced to research opportunities

STTP COURSE CONTENTS

- Advanced VLSI System design
- VLSI device modeling
- Design and verification
- Mixed signal design
- FinFET technology
- Memristors
- FPGA based Design & Implementation
- ASIC design
- Challenges in emerging VLSI
- Research areas in VLSI
- Advanced HDLs & their advantages
- Hands on Lab sessions
- Hands on usage of CAD tool for Custom IC design

Resource Persons

Eminent faculty from IITs, NITs, IIITs , reputed Universities /colleges and industry experts

Address for Communication

Sri O. Anjaneyulu,
Associate Professor,
Dept. of EIE
+91-9440591120
oa.eie@kitsw.ac.in

Sri B. Jeevan,
Assistant Professor,
Dept. of EIE
+91-9912155777
bj.eie@kitsw.ac.in